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EXAMINER	
ZARABIAN, A	
ART UNIT	**PAPER NUMBER**
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DATE MAILED: 01/11/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1-36 are pending in the application.
   Of the above, claims 6-8 and 34-36 are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-5 and 9-33 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☒ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☒ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☒ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

Applicant's election of claims 1-5 and 9-33 in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (M.P.E.P. § 818.03(a)).

Claims 34-36 recite more than one invention. Upon allowance of claim 12 rejoinder of claims 34-36 with be permitted.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: In claims 12, line 10, before "memory", "said" should be added, in line 12, "the" should be replaced with "a". In claim 16, line 10, "mode" should be replaced with "node". Appropriate correction is required.

Claims 2, 4, 9, 11 and 12-33 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, lines 10 and 13, "data output terminals", it is not clear if these are the same terminals as in claim 2, line 5.

In claim 4, line 7 and claim 9, line 7 "said memory cells" has no antecedent basis.

In claim 11, line 15, "said latch means" has multiple antecedent basis (first and second latch means).

In claim 12, lines 13-14, "by which said data output means can externally supplied at a time" is vague. Clarification is required.

In claim 16, lines 11 and 20, "in parallel with other" is vague. Clarification is required.

In claim 16, lines 19 and 22, "the second fixed potential node" and "said first fixed potential" has no antecedent basis.

In claim 24, line 2, "said comprising units" has no antecedent basis.

In claim 32, lines 2 and 3, "the set of means associated with" and "the set of additional means" have no antecedent basis.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claim 9 is rejected under 35 U.S.C. § 103 as being unpatentable over Ueoka in view of An.

Ueoka in figures 1 and 2 discloses a memory device having pulsed clock signal (fig. 4) comprising a plurality of banks (11) including memory arrays, activating means for simultaneously activating plurality of bank in a test mode (Abst), but Ueoka does not teach the use of a precharging means. An in figure 4 teaches the use of precharge means for precharging memory arrays on a bank by bank basis. Therefore it would have been obvious to one of ordinary skill in the art to precharge the memory arrays of Ueoka on a bank by bank basis, as taught by An, for precharging the bit lines of Ueoka.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 and 12 rejected under 35 U.S.C. § 102(e) as being anticipated by Adams.

Adams in figure 1 discloses a memory device responsive to a clock signal comprising; a memory cell array having plurality of cells (14), selection means (16) for selecting the memory cells, read means for reading the data and compressing means (32)

responsive to a test made for compressing the data indicating the defective memory and outputting data to output terminal (see col. 3, lines 22-27).

Claims 2, 3, 13, 14, 31, 32 and 33 are rejected under 35 U.S.C. § 103 as being unpatentable over Adams.

Adams as applied in prior rejection discloses every claimed subject matter except the use of plurality of elements, output buffers and read registers. The use of output buffers and read registers is well known in the art and use more than one array (including read, select and compress means) instead of the single array shown in Adams would have been obvious to one of ordinary skill in the art at the time the invention was made in order to test more than one array for faulty elements. Activation of plurality of memory blocks in a test mode is well known in the art.

Claims 4 and 5 are rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Getzlaff in view of An.

Adams as applied in prior rejection discloses every claimed subject matter except the use of a precharger and a subcompressor.

Getzlaff shows a compressor having smaller subcompressors. An as disclosed in prior rejections teaches the use of a precharger. Therefore it would have been obvious to one of ordinary skill in the art at the time invention was made to use a

precharger, such as An's; to charge the bitlines and to use a two stage compress, such as Geltzlaff's, in place of data compressor (32) of Adams in order to compress the data.

Claim 10 is rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Getzlaff.

Adams as applied in prior rejection discloses a read means (16, 18..) for reading data of memory cells into a data compressor (32), but Adam does not teach the details of the compressor. Getzlaff as applied in prior rejection in figure 5A teaches the use of a compressor having a first wired circuit having a gate receiving a data read signals (C1,D1) and being connected in parallel to a first signal (GND), a second wired circuit having p-channel FET, receiving read signals (Bo, B1) and being coupled in parallel to a second signal (VDD). The outputs of the wired circuits are connected to logic means. Therefore it would have been obvious to one of ordinary skill in the art to use the compressor of Getzlaff in place of data compressor (32) of Adams in order to compress the data read from the memory cell array.

Claims 11 and 15-30 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.

The prior art does not disclose a generation means responsive to prechargable signal (as in claim 16) and the

relationship between prescribed number of data registers and predetermined number of memory cells (as in claims 19 and 29).

Any inquiry concerning this communication should be directed to A. Zarabian at telephone number (703) 308-4905.

A. Zarabian
Exr. Av. 2511

Zarabian/tj

Jan. 6, 1995